1. A method comprising:

detecting that a processor's frequency has changed in response to processor cooling; and

generating an interrupt in response to the detection of the frequency change.

2. The method of claim 1 including providing an interrupt to an operating system.

3. The method of claim 1 including reading the performance state of the processor in response to the interrupt.

4. The method of claim 3 including determining a new performance state.

5. The method of claim 4 including scheduling a bandwidth allocation.

6. The method of claim 2 including setting up a periodic timer.

7. The method of claim 6 including monitoring the processor temperature at periodic intervals.

8. The method of claim 1 including detecting a high temperature or a low temperature interrupt and reading the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

9. The method of claim 1 wherein detecting a frequency change includes detecting a processor phase locked loop event.

10. The method of claim 1 including using hardware controlled throttling.

11. An article comprising a medium storing instructions to enable a processor-based system to:

detect that a processor's frequency has changed in response to processor cooling; and

generate an interrupt in response to the detection of the frequency change.

12. The article of claim 11 further storing instructions to enable a processor-based system to provide an interrupt to an operating system.

13. The article of claim 11 further storing instructions to enable a processor-based system to read the performance state of the processor in response to the interrupt.

14. The article of claim 13 further storing instructions to enable a processor-based system to determine a new performance state.

15. The article of claim 14 further storing instructions to enable a processor-based system to schedule a bandwidth allocation.

16. The article of claim 12 further storing instructions to enable a processor-based system to set up a periodic timer.

17. The article of claim 16 further storing instructions to enable a processor-based system to monitor the processor temperature at periodic intervals.

18. The article of claim 11 further storing instructions to enable a processor-based system to detect a high temperature or a low temperature interrupt and read the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

19. The article of claim 11 further storing instructions to enable a processor-based system to detect a processor phase locked loop event.

20. The article of claim 11 further storing instructions to enable a processor-based system to use hardware controlled throttling.

21. A system comprising:

a processor;

a temperature sensor coupled to said processor; and

a storage storing instructions that enable the processor to detect that the processor's frequency has changed in response to processor cooling and generate an interrupt in response to detection of the frequency change.

22. The system of claim 21 including a storage storing an operating system, said interrupt being provided to the operating system.

23. The system of claim 21 wherein said storage stores instructions that enable the processor to read the performance state of the processor in response to an interrupt.

24. The system of claim 21 wherein said processor determines a new performance state.

25. The system of claim 24 wherein said storage stores instructions that enable the processor to schedule a bandwidth allocation.

26. The system of claim 22 wherein said storage stores instructions that enable the processor to set up a periodic timer.

27. The system of claim 26 wherein said storage stores instructions that enable the processor to monitor the processor temperature at periodic intervals.

28. The system of claim 21 wherein said storage stores instructions that enable the processor to detect a high temperature or a low temperature interrupt and read the processor performance state in response to the detection of a high temperature or a low temperature interrupt.

29. The system of claim 21 wherein said storage stores instructions that enable the processor to detect a processor phase locked loop event.

30. The system of claim 21 including hardware controlled throttling.